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U1S S2212

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GB 2235340 A GB 2220538 A GB 2089578 A
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15th EUROPEAN MICROWAVE CONFERENCE PROCEEDINGS, 9-13 Sept 85 D.Levy et al. A broadband hybrid switchable combiner, pp 629-634 see figure 2 and description thereof

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(54) An r.f. switch using transistors as switch and gain elements

(57) A controlling circuit 35 biases one of transistors BJT1 and BJT2 to block the incoming signal and the other into the gain region. Further transistors may be used. The arrangement may be used for switching satellite signals.

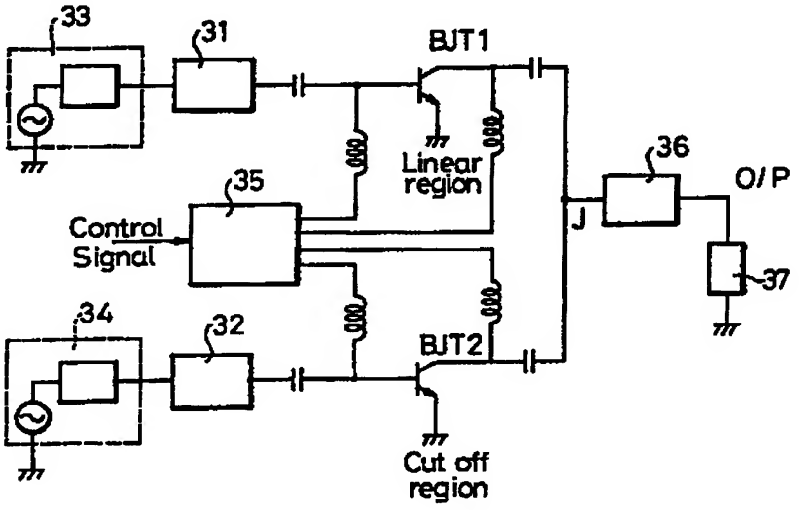

Fig. 2

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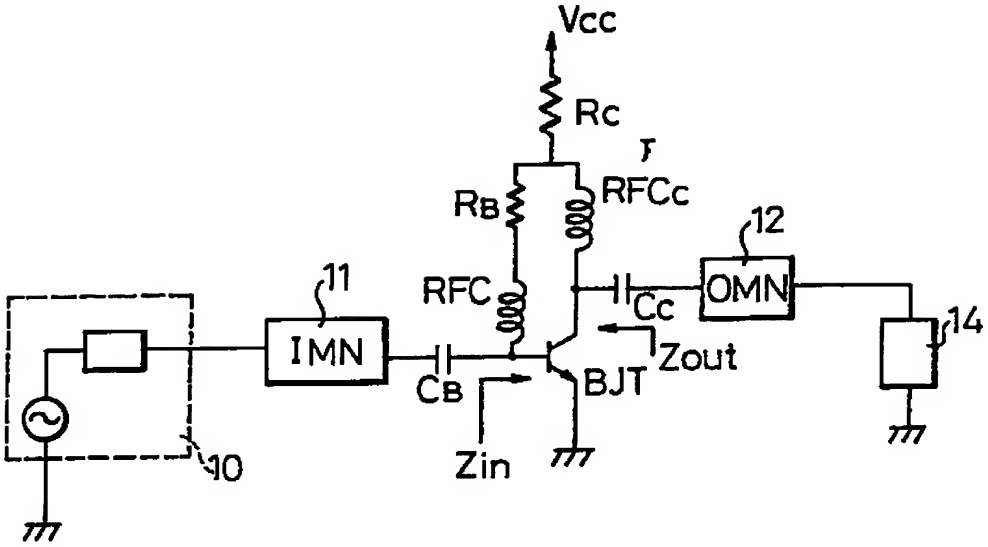

Fig. 1

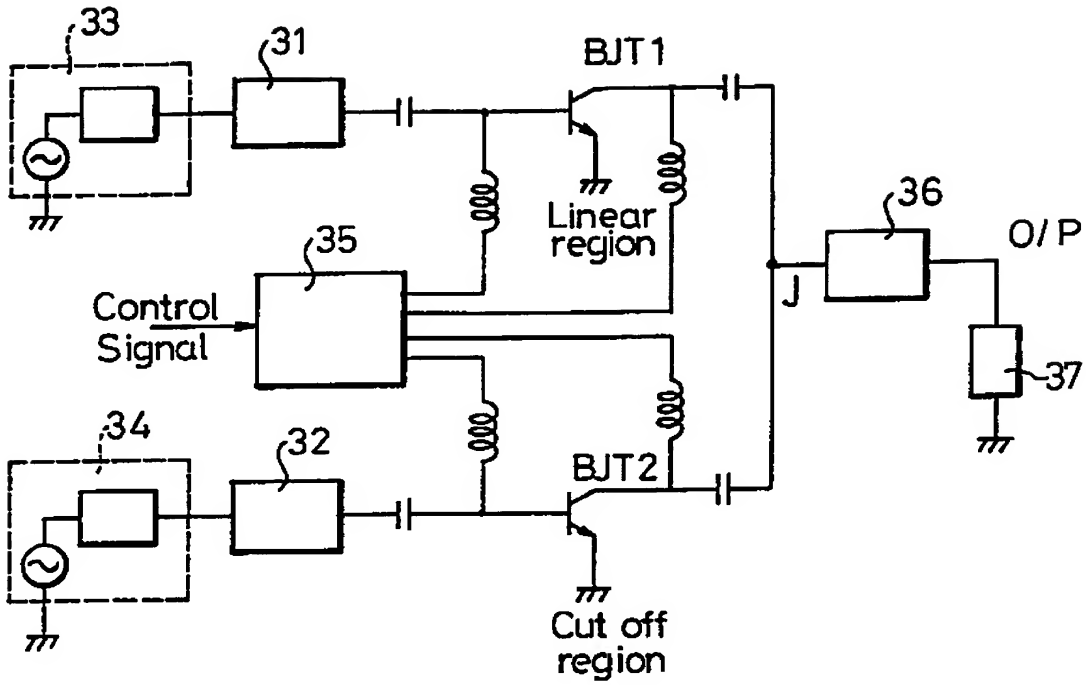
33
31
BJT1
Linear region
36
O/P
35
Control Signal
J
37
34
32
BJT2
Cut off region

Fig. 2

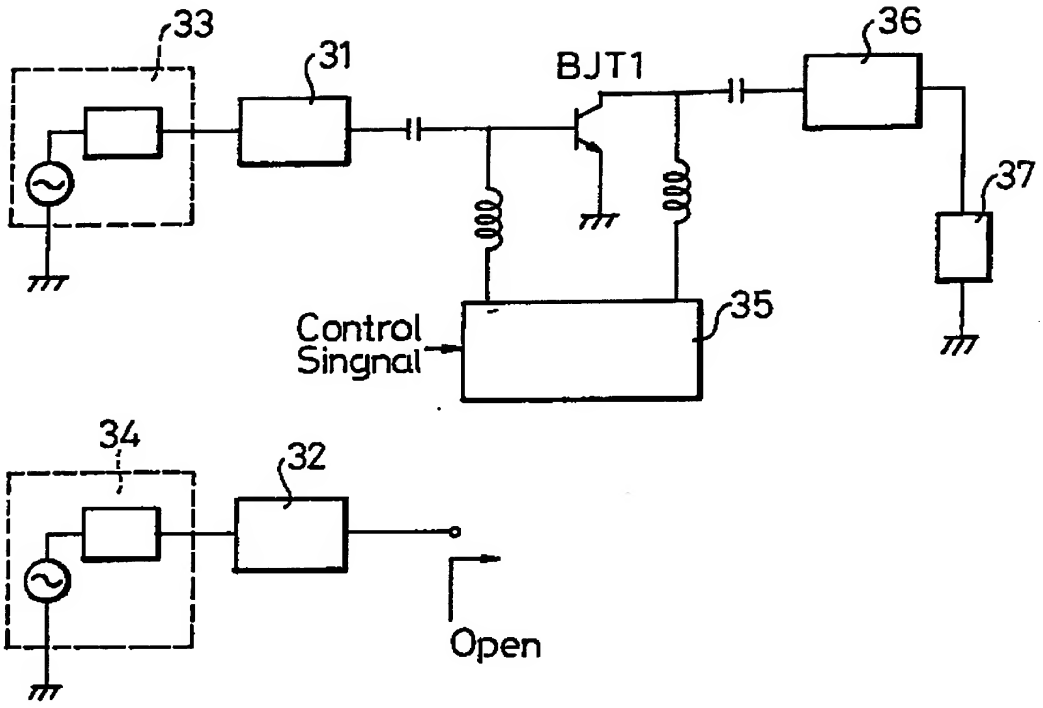

Fig. 3

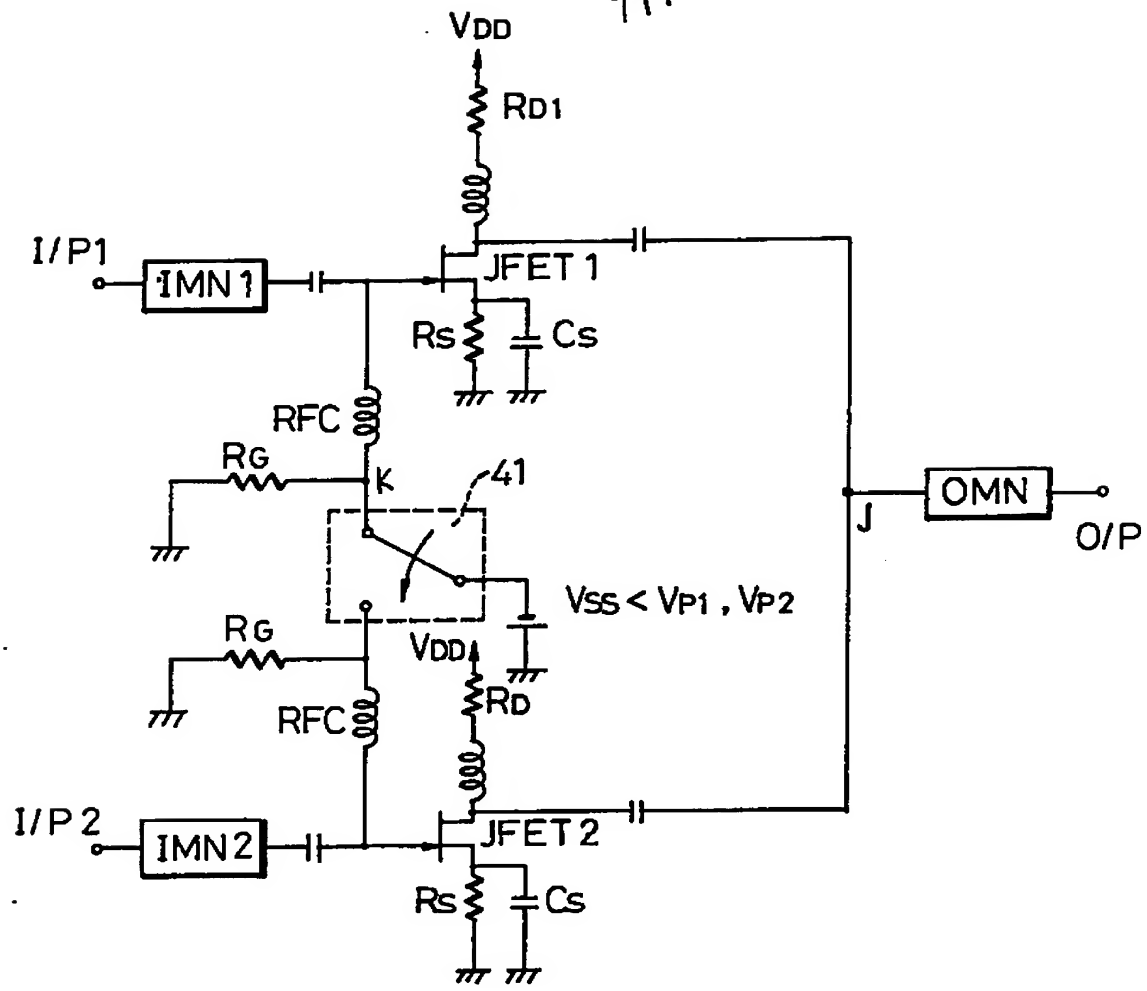
VDD
RD1
I/P1
IMN1
JFET 1
RS
CS
RFC
RG
K
41
J
OMN
O/P
VSS < VP1 , VP2
RG
VDD
RD
RFC
I/P 2
IMN2
JFET 2
RS
CS

Fig. 4

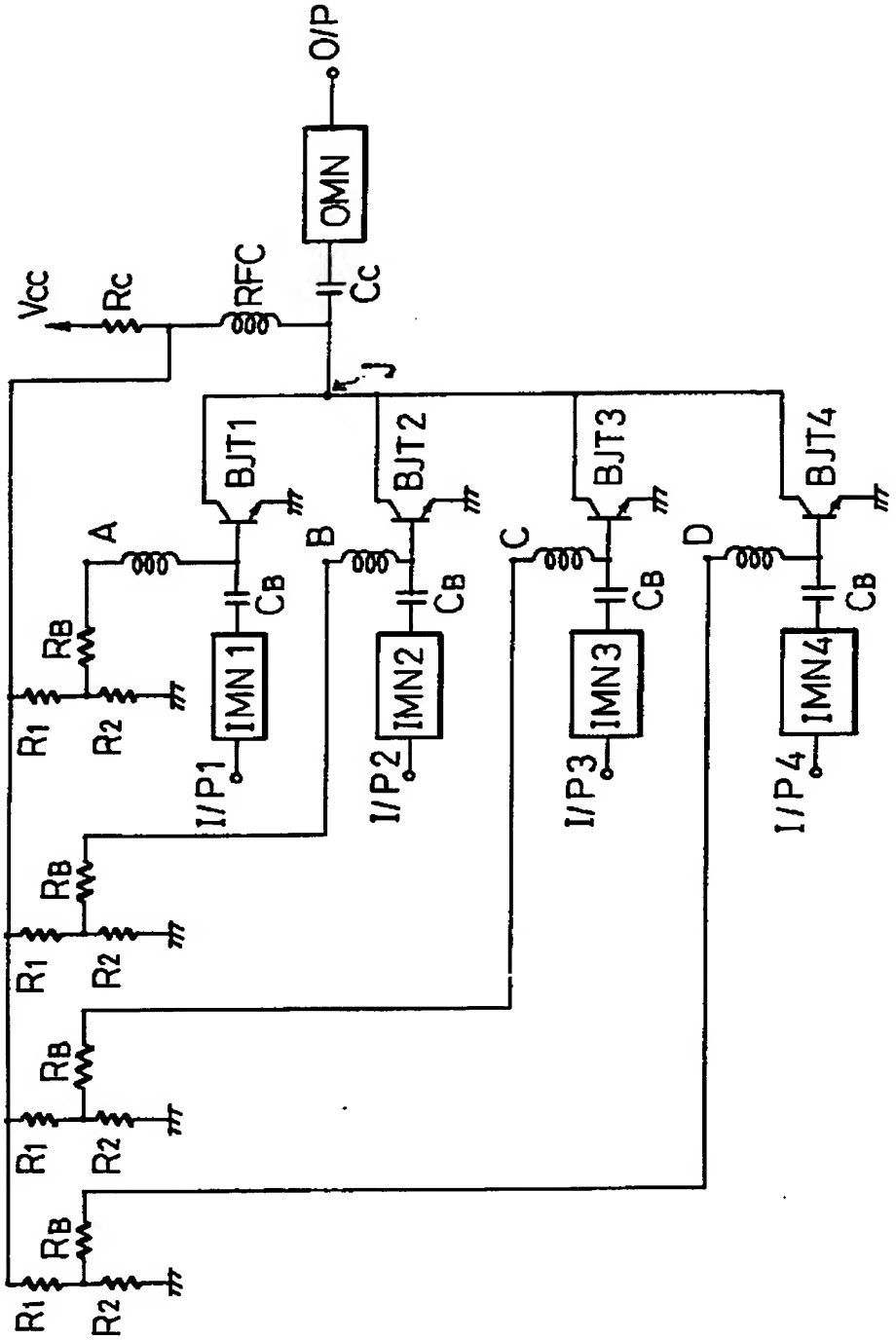
O/P
OMN
Cc
RFC
Rc
Vcc
J
BJT1
BJT2
BJT3
BJT4
A
B
C
D
CB
IMN1
IMN2
IMN3
IMN4
I/P1
I/P2
I/P3
I/P4
RB
R1
R2

Fig. 5

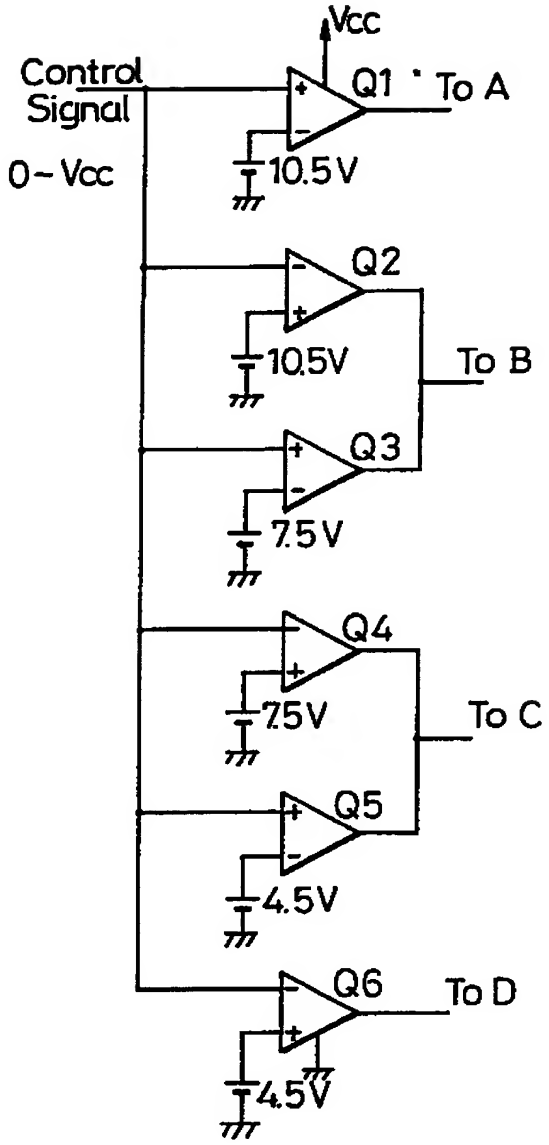
Vcc
Control Signal
0 - Vcc
Q1
To A
10.5V
Q2
10.5V
To B
Q3
7.5V
Q4
7.5V
To C
Q5
4.5V
Q6
To D
4.5V

Fig. 6

Control Voltage	0 ~ 4.5V	4.5V ~ 7.5V	7.5V ~ 10.5V	10.5V ~ Vcc
A	0	0	0	1
B	0	0	1	0
C	0	1	0	0
D	1	0	0	0

1 = V_{BE} ON ≈ 0.7V BJT ON

0 = V_{CE} SAT ≈ 0.2V BJT OFF

Fig. 7

TITLE: HIGH FREQUENCY SINGLE-POLE MULTIPLE-THROW SWITCH WITH GAIN PERFORMANCE

BACKGROUND OF THE INVENTION

The present invention relates to a high frequency single-pole multiple-throw switch with gain performance and more particularly to the circuit of a single-pole multiple-throw switch composed of transistors.

The switch of the present invention is particularly suitable for switching vertical and horizontal polarized satellite signals. The currently common switching elements used in switching or selecting high frequency signals are relays or PIN diodes. In the case of utilizing the relay as the selection switch, however, since the relay is a mechanical elements, it will has higher failure rate and shorter life-span, in comparison with the electronic elements, when the temperature is too high or too low. Besides, since relay is a passive element, it can not provide any gain to the signals. The utilization of the PIN diode as the selection switch can avoid the problems of high failure rate and short lifetime as presented in the utilization of the relay. However, it requires more elements to achieve same degree of signal isolation (4 to 8 PIN diodes are usually needed to achieve 20 dB isolation in UHF for a switch). In addition, such type of circuits will usually cause signal loss and therefore can not provide gain, either.

SUMMARY OF THE INVENTION

One object of the present invention is to provide a reliable and long-life selection switching circuit with less elements, simple circuit structure and gain performance which utilizes transistors as the switching elements. The signal selection is controlled by

switching the operating bias voltages of the transistors to make the transistors operated in a linear region or a cutoff region. The present invention also makes a deliberated arrangement for the matching network that is necessary for the input and output of the transistors to be connected such that the structure of the switching circuit becomes simpler and the design of this type of circuit is easier. Furthermore, since such transistors are cheaper elements with gain performance, extra amplifiers are not needed to compensate the signal loss in the circuit of the present invention. Therefore, the cost of the circuit can be further reduced.

These and other objects, advantages and features of the present invention will be more fully understood and appreciated by reference to the written specification.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an illustrated diagram of a general circuit which uses BJTs (bipolar junction transistors) as amplification elements;

Fig. 2 is a circuit block diagram of a first embodiment of a single-pole multiple-throw switch circuit in accordance with the present invention;

Fig. 3 is an equivalent circuit diagram of the circuit shown in Fig. 2;

Fig. 4 is a circuit block diagram of a second embodiment of a single-pole multiple-throw switch circuit in accordance with the present invention;

Fig. 5 is a circuit block diagram of a third embodiment of a single-pole multiple-throw switch circuit in accordance with the present inventi n;

Fig. 6 is a diagram circuit of the input voltages of the circuit shown in Fig. 5; and

Fig. 7 is a table showing the relationship of the input voltages and the outputs of respective terminals A -- D in Figs. 5 and 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Now please refer to Fig. 1 which illustrates a circuitry diagram using bipolar junction transistors (BJTs) as amplifying elements. As shown in this figure, in order to make a signal source 10 match with the input port of the transistor and make a load 14 match with the output port of the transistor, it is necessary to connect the input port and the output port of the transistor BJT respectively through an input matching network 11 and an output matching network 12 to obtain performance expected. Capacitors C_B and C_C are respectively used as DC blocking capacitors on the input and output ports of the BJT. The purpose of these capacitors is to prevent the base voltage V_B and the collector voltage V_C of the BJT from being affected by the input and output matching networks 11 and 12. Radio frequency chokes (RF chokes) RFC_B and RFC_C are used in preventing AC signals from being affected by the DC circuit of Fig. 1. Parameters Zin and Zout represent the input impedance and the output impedance of the BJT, respectively.

Those who are skilled in this art may use other bias circuits or change the values of C_B, C_C, RFC_B and RFC_C to turn them into part or all of the matching networks to reduce the number of the elements of the matching networks.

Further, the type of BJT has a characteristic that when the bias voltage thereof falls within the linear region of the V (voltage) - I (current) characteristic diagram, such a transistor has an amplification

function for high frequency and has specific input and output impedance Zin and Zout. While in the cutoff region of the V-I curve, the transistor has no longer the amplification function and the impedances Zin and Zout will approach to infinite (it is because when the p-n junction of the BJT is reverse biased, the reverse saturation current flowing through the junction is very small and the impedance Z = V /I).

Accordingly, the present invention utilizes the above characteristics of the bipolar junction transistors, i. e., the transistor amplifies the signals when its operation region falls within the linear region, while in the cutoff region, the impedance Zin and Zout are extremely high, to design a switching circuit. As most of the manufacturers of high frequency transistors today are able to effectively control the quality of the transistors so that the parameters required for the transistors do not carry large deviation during mass production. Therefore, the switching circuit of the present invention will not have large quality deviation during the mass production.

In designing the high frequency switching circuits, on one hand, it requires a good impedance matching between the input port and the signal source and between the output port and the load when the signals are passing to reduce signal loss. Using transistors as signal-passing elements, in the condition of good signal matching, can not only eliminate the signal loss but also provide a gain to the signal. On the other hand, the transistors are able to reject unwanted signals so as to have a good signal isolation when it is cut-off. By using the characteristic of transistors of providing a high impedance in the cutoff region, a mismatch manner between the signal source and the switching circuit can

be achieved so that the reflected signals can be prevented from entering the switching circuit.

It can also add a switch between the switching circuit and the signal source of the present invention so that when the transistor of the present invention is cutoff, the signal source will be switched to a dummy load to eliminate the mismatch of the signal source. Such a technique is also falling within the scope of the present invention.

Another special feature of the present invention resides in that, as shown in Fig. 2 and 5, the present invention uses a plurality of transistors (BJT1 and BJT2 in Fig. 2 and BJT1 -- BJT4 in Fig. 5) as switching elements, each of which connects with a respective input matching network (31 and 32 in Fig. 2 and IMN1 -- IMN4 in Fig. 5), and there is only one signal output matching network (element 36 in Fig. 2 and OMN in Fig. 5) connecting with the outputs of all of the transistors. It is because that if each transistor has its own independent output matching network, there will be interference between individual output matching networks and it will be difficult to compute the values of elements in each matching network. The present invention utilizes the characteristic of the transistor which provides high output impedance in the cutoff region, and ensures that only one transistor is in the operation regions at one time and connects the output of each transistor to a common junction (junction J as shown in Figs. 2, 4 and 5). Therefore, the output impedance at the junction J of the switching circuit of the present invention will be very close to that of a single transistor so that only the parameters of one of the transistors have to be considered in designing the output matching network 36. Another advantage of the present invention is that the number of the elements

desired in the matching circuit is reduced so as to save the space and cost of the switching circuit.

In the embodiment of Fig. 2, when the transistor BJT1 is operating in the linear region and the transistor BJT2 is in the cutoff region, by means of various bias voltage controlled by a bias voltage controlling circuit 35, the circuit of Fig. 2 will be equivalent to that of Fig. 3. At this situation, the input and output of the transistor BJT2 are deemed as open. Therefore, on one hand, the signal from the signal source 33 can enters the input matching network 31 and is amplified by the transistor BJT1 and then is coupled into the load 37 via the output matching network 36 without being affected by the another transistor BJT2. On the other hand, the signal from the signal source 34 is reflected back by the transistor BJT2 and can not be amplified by the transistor BJT2. In this manner, the switching circuit of the present invention can amplify the desired signals and reject the unwanted signals which is function as a high frequency single-pole double-throw switch with good signal isolation.

Fig. 4 shows a second embodiment of the present invention, in which N-channel JFET (JFET1 and JFET2) is used as amplifying elements and a switch 41 instead of the bias voltage controlling circuit 35 in Fig. 2 is used to control the bias voltage. It should be noted that bias voltage Vss is a negative voltage which is lower than the pinch-off voltages V_{P1} and V_{P2} of both JFET1 and JFET2. When the switch 41 connects the Vss to the gate DC inserting point (K point in Fig. 4) of the JFET1 (as the connection shown in Fig. 4), the JFET1 enters into the cutoff region and stop amplifying the signal coming from the signal source I/P1. At the time, the signals coming from the source I/P2 enters into the transistor JFET2 via an input matching network

IMN2 and are amplified by the transistor JFET 2 and output to an output matching network OMN without interference by the signals from the signal source I/P1.

The JFETs used in the above embodiment are self-biased and it should be easy for those who are skilled in this art to find out the values of the parameters of R_D, R_G, R_S and C_S for biasing the JFET to the required operation region.

Fig. 5 shows the connection and the control method of a single-pole quadruple-throw switching circuit using BJTs as switching elements. In this figure, points A, B, C and D represent the respective base DC inserting point of the switching elements BJT1 -- BJT4. Due to the RF choke RFC, the DC voltages inserting into these points have good isolation and do not effect the high frequency AC signal. If the voltage on any one of these points drops below the base-emitter turn-on voltage V_{BE} (typical 0.7 V), the BJT transistor corresponding to this point will be cutoff.

The switching circuit of Fig. 5 uses five voltage comparators Q1-Q5 to control the voltages input to the transistors BJT1 -- BJT4, as shown in Fig. 6. The present invention is designed according to the characteristic of the active push-down function of the voltage comparator which is opened when disabled and is grounded when enabled so that only one BJT is in the linear region and the rest of the BJTs are in the cutoff region when any voltage in the range of 0 - Vcc is input. The relationship of the control voltages and the transistors is as shown in the table of Fig. 7. Further, the voltage comparator commomly-used in the present invention is the commerical-used comparator No. LM 339.

In addition to being the bias resistors of the BJT, the resistors R1 and R2 in Fig. 5 are also the pull-up resistors of the comparators Q1 ~ Q6.

When two or more active push-down elements are connected to a pull-up resistor and when one of which is enabled, the voltage at the junction will become Low. This kind of circuit configuration is called wire-AND connection. The comparators Q2, Q3, Q4 and Q5 in Fig. 6 are connected in the wire-and configuration.

The present invention may be connected by the wire-AND configuration as shown in Fig. 6 to achieve a more flexible control circuit such that each BJT can be controlled by multiple active push-down elements and each active push-down element can interface with various switches, transducers and logic circuits. In comparison with the well known circuits with relays and PIN diodes, the present invention is easier to interface with external devices.

The single-pole quadruple-throw switch of Fig. 5 of the present invention has great commercial value in the distribution of satellite television signals. Since the bandwidth of the home satellite receiver is limited and the number of satellites and the programs are increasing day after day, some additional coaxial cables may be needed for each satellite to transmit the satellite signal to the subscriber after the signal frequency is block down converted by a low noise block down converter. The cost in this case, however, will be too high. Besides, most of the current satellite subscribers only use one coaxial cable to connect the outdoor antennas (more than two antennas). Therefore, the reasonable approach is to switch various satellite signals by a multiple-port high frequency switch. The single-pole multiple-throw high frequency switch according to the present invention is exactly the best

selection. The present invention has the following advantages:

(a) The circuit provide a gain to compensate the signal loss and has good signal isolation;

(b) The circuit has a higher reliability and a longer lifetime in comparison with the conventional circuit with relays;

(c) The circuit needs less elements (in comparison with the circuit with PIN diodes) and the circuit structure is much simpler since the circuit needs not compensation amplifiers and only one output matching network is needed;

(d) The cost of the circuit is low; and

(e) The circuit is easy to be interfaced with various control signals since each BJT is controllable by the wire-AND connection.

It can construct a multiple-pole multiple-throw switching circuit by combining a number of single-pole multiple-throw switching circuits of the present invention. Of course, the multiple-pole multiple-throw switching circuit will not depart from the scope of the present invention.

As various possible embodiments might be made of the above invention without departing from the scope of the invention, it is to be understood that all matter herein described or shown in the accompanying drawing is to be interpreted as illustrative and not in a limiting sense. Thus it will be appreciated that the drawings are exemplary of a preferred embodiment of the invention.

CLAIMS

1. A high frequency single-pole multiple-throw switch, comprising:

a plurality of input ports;

a plurality of switching means having the same number as the input ports; each comprising:

an input matching network connected with one of the input ports; and

a transistor of which an input electrode is connected with the output of the input matching network;

a junction connecting all outputs of the transistors of the switching means together;

a single output matching network being coupled by said junction; and

a DC voltage biasing network for providing bias voltages for respective transistors so that when switching a certain input signal, only one of the transistor is operated in a linear region and the other transistors are operated in cutoff regions.

2. A high frequency single-pole multiple-throw switch as claimed in Claim 1, wherein said transistors are bipolar junction transistors and are arranged as a common emitter mode.

3. A high frequency single-pole multiple-throw switch as claimed in Claim 2, further comprising a plurality of active push-down elements each connected to a DC inserting point of the base of either of the transistor, wherein one or more push-down elements are used to push the base voltages of the transistors down below forward operating bias voltages thereof so as to force the transistors to operate in the cutoff region.

4. A high frequency single-pole multiple-throw switch as claimed in Claim 1, 2 or 3, being used for switching a number of different satellite signals to a satellite signal receiver.

5. A high frequency single-pole multiple-throw switch substantially as hereinbefore described with reference to, and as illustrated in, Figures 2 and 3, or Figure 4, or Figures 5 and 6, of the accompanying drawings.

12

Patents Act 1977 Examiner's report to the Comptroller under Section 17 (The Search report)	Application number GB 9410296.9
Relevant Technical Fields (i) UK Cl (Ed.M) H3W (WGA) (ii) Int Cl (Ed.5) H03F 3/60, 3/72, 3/68	Search Examiner D MIDGLEY Date of completion of Search 28 JULY 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE DATABASES: WPI	Documents considered relevant following a search in respect of Claims :- 1-5

Categories of documents

X:	Document indicating lack of novelty or of inventive step.	**P:**	Document published on or after the declared priority date but before the filing date of the present application.
Y:	Document indicating lack of inventive step if combined with one or more other documents of the same category.	**E:**	Patent document published on or after, but with priority date earlier than, the filing date of the present application.
A:	Document indicating technological background and/or state of the art.	**&:**	Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X, Y	GB 2235340 A	(FUNAL) see Figure 4 and description thereof	X: 1-2, 4 Y: 5
X, Y	GB 2220538 A	(MARCONI) see Figure 1 and description thereof	X: 1-2, 4 Y: 5
Y	GB 2089578 A	(PIONEER) see Figure 4 and description thereof	5
X, Y	WO 92/22937 A1	(CAMBRIDGE) whole document	X: 1-2, 4 Y: 5
X, Y	15th European microwave conference proceedings; 9-13 September 1985. D Levy et al. A broad band hybrid switchable combiner pages 629 to 634. See Figure 2 and description thereof.		X: 1-2, 4 Y: 5

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